CLAIMS

WHAT IS CLAIMED:

1. A semiconductor device, comprising:

a substrate, said substrate having a surface;

a first recess and a second recess formed in said substrate, said first recess having a first width and extending a first depth beneath the surface of said substrate, said second recess having a second width and extending a second depth beneath the surface of said substrate;

said first width of said first recess being greater than said second width of said second recess;

said second depth of said second recess being greater than said first depth of said first recess; and

an isolation structure positioned in at least a portion of said first and second recesses.

2. The device of claim 1, wherein said isolation structure is comprised of a single isolation material.

3. The device of claim 1, wherein said isolation structure is comprised of a plurality of spacers formed in said first recess.

4. The device of claim 1, wherein said isolation structure is comprised of an isolation liner positioned in at least a portion of at least one of said first and second recesses.

5. The device of claim 1, wherein said isolation structure is comprised of:

a plurality of spacers positioned in said first recess;

an isolation liner positioned in at least a portion of said second recess; and

an isolation material positioned between said spacers and in said second recess adjacent said isolation liner.

6. The device of claim 1, wherein said isolation structure comprises:

a plurality of spacers positioned in said first recess;

an isolation liner positioned in said second recess and extending between said spacers; and

an isolation material positioned in said first and second recesses between said isolation liner.

7. The device of claim 1, wherein said isolation structure is comprised of silicon dioxide.

8. The device of claim 1, wherein said isolation structure is comprised of oxynitride.

9. The device of claim 3, wherein said spacers are oxide spacers.

10. The device of claim 3, wherein at least one of said spacers is an oxynitride spacers.

11. The device of claim 4, wherein said isolation liner is comprised of at least one of the group of tetraethyl orthosilicate, oxide, oxynitride or nitride.

12. The device of claim 1, wherein said first depth of said first recess ranges between approximately 500-1000 Å beneath the surface of said substrate.

13. The device of claim 1, wherein said second depth of said second recess extends approximately 1500-4000 Å beneath the surface of said substrate.

14. The device of claim 2, wherein said first width of said first recess ranges between 2000-3000 Å.

15. The device of claim 2, wherein said second width of said second recess ranges between 1400-2000 Å.

16. A semiconductor device, comprising:

a substrate, said substrate having a surface;

a first recess and a second recess formed in said substrate, said first recess having a first width and extending a first depth beneath the surface of said substrate, said second recess having a second width and extending a second depth beneath the surface of said substrate;

said first width of said first recess being greater than said second width of said second recess;

said second depth of said second recess being greater than said first depth of said first recess; and

an isolation material positioned in at least a portion of said first and second recesses.

17. The device of claim 16, further comprising a plurality of spacers positioned in said first recess.

18. The device of claim 16, further comprising an isolation liner positioned in at least a portion of said second recess, at least a portion of said isolation liner positioned between said spacers and said isolation material.

19. A semiconductor device, comprising:

a substrate, said substrate having a surface;

a first recess and a second recess formed in said substrate, said first recess having a first width and extending a first depth beneath the surface of said substrate, said second recess having a second width and extending a second depth beneath the surface of said substrate;

said first width of said first recess being greater than said second width of said second recess;

said second depth of said second recess being greater than said first depth of said first recess; and

an isolation structure, said isolation structure comprising:

a plurality of spacers positioned in said first recess;

an isolation liner positioned in said second recess and adjacent said spacers; and

an isolation material positioned in said first and second recess, said isolation material being positioned adjacent said isolation liner.

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20. A method for forming an isolation trench in a semiconductor substrate, said substrate having a surface, comprising:

forming a first recess in said substrate, said first recess having a first width and extending a first depth beneath the surface of said substrate;

forming a second recess in said substrate, said second recess having a second width that is less than said first width of said first recess, said second recess extending a second depth beneath the surface of said substrate, said second depth being greater than said first depth of said first recess; and

forming an isolation structure in said first and second recesses.

21. The method of claim 20, wherein forming an isolation structure comprises forming at least one material in at least one of said first and second recesses.

22. The method of claim 20, wherein forming an isolation structure comprises forming a single material in said first and second recesses.

23. The method of claim 20, wherein forming an isolation structure comprises forming at least two different materials.

24. The method of claim 20, wherein forming said isolation structure comprises:

forming a plurality of spacers in said first recess;

forming an isolation liner in at least a portion of said second recess; and

forming an isolation material in said second recess adjacent said isolation liner, at least a portion of said isolation liner extending between said spacers and said isolation material.

25. The method of claim 20, wherein forming a first recess comprises etching said first recess.

26. The method of claim 20, wherein forming said second recess comprises etching said second recess.

27. The method of claim 20, wherein forming an isolation material comprises depositing said isolation material in said second recess.

28. A method for forming an isolation trench in a semiconductor substrate, said substrate having a surface, comprising:

forming a first recess in said substrate, said first recess having a first width and extending a first depth beneath the surface of said substrate;

forming a second recess in said substrate, said second recess having a second width that is less than said first width of said first recess, said second recess extending a second depth beneath the surface of said substrate, said second depth being greater than said first depth of said first recess;

forming a plurality of spacers in said first recess;

forming an isolation liner in at least a portion of said second recess; and

forming an isolation material in said second recess adjacent said isolation liner, at least a portion of said isolation liner extending between said spacers and said isolation material.